Edge and Bevel Automated Defect Inspection for 300mm Production Wafers in Manufacturing

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Abstract
In this paper, we describe a solution for wafer edge and bevel apex defect inspection for a 300mm semiconductor automated fab. Traditionally, we have used an advanced macro inspection solution for topside wafer inspection. The automated tool revealed that defects surfacing after the back end of line (BEOL) copper chemical mechanical polish planarization (Cu CMP) process were significantly impacting yields. We suspected that particles and film on the edge and bevel were flaking off on to the top of the wafers, causing the yield degradation. However, we needed more information from the edge to confirm our hypothesis. Since offline manual edge analysis was not cost-effective for larger wafer sampling, we sought to develop an inline bevel inspection at the CMP sector that was fast, cost-effective, and integrated with the advanced macro inspection tool. We also established a long-term goal of expanding the process into an all-surfaces inspection within one manufacturing operation step.

This paper describes how we integrated the top-down macro and edge bevel inspection into a single automated operation, enhancing data collection and our ability to take corrective action. The process includes full top and complete edge bevel inspection of less than 10 percent of each lot. Although we ran sample tests to inspect edges after numerous processes, this paper focuses on BEOL Cu CMP inspection, including data collection and corrective actions. We also highlight the benefits of edge inspection, and the new level of automated process control.

As a result of edge inspection, we have taken corrective actions that have reduced defects on the edge bevel, and improved wafer final test yields by 10 percent from the baseline.

Keywords
Wafer edge bevel apex inspection

INTRODUCTION
Traditionally, the wafer edge has been of secondary concern to semiconductor manufacturers, since it was considered a non-active area. However, there is a growing industry awareness that wafer edge and backside conditions impact yields, directly and indirectly. For instance, a scratch on the bottom of a wafer can cause a hot spot on the top. A large scratch or residual slurry on the bevel can flake or peal off, depositing particles on the topside that cause defects.

Data collected by advanced macro inspection showed that defects formed after Cu CMP were among our top five yield inhibitors. Manual analysis showed that film depositions on the edge were fairly thick after Cu CMP. We suspected that the edge condition—such as copper overflow—might be causing the majority of post-Cu CMP defects: the thicker film layers would have a greater tendency to delaminate and flake off onto the wafer surface.

If edge defects were affecting yields, we could remedy the issue by performing a clean after appropriate processes. Determining which cleaning chemicals to use, and knowing when to perform the clean would require more information from the edge.

Although our advanced macro system could detect defects down to 0.5 microns on the topside and top edge of the wafer, the system could not inspect the side or bottom edge. Manual inspection could view all sides of the edge, but it was not a cost-effective method for inspecting large numbers of wafers. An inline edge normal bevel inspection at the Cu CMP sector, however, would monitor bevel edge defects, and uncover any correlation between the edge and yield-detracting defects.

We did not want to implement a standalone edge inspection module, since it would accrue additional wafer delivery, load, and align time—increasing the total cost of ownership. However, we found we could integrate the E20™ edge inspection module from August Technology with our AXi™ Series advanced macro inspection tool to perform top-down macro and edge bevel inspection in a single automated operation.

THE INSPECTION TECHNOLOGY
The E20 performs a comprehensive edge inspection, including the edge top, edge normal, and edge bevels. To achieve a complete edge inspection, the module captures

color images from both above the wafer (top view) and from the side view (edge normal), as shown in Figure 1.

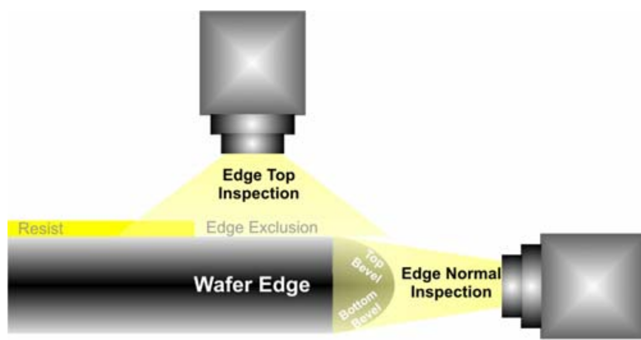

Figure 1. Edge inspection

The inspection algorithm uses a dynamically created model to detect anomalies on the top and side of the wafer edge. Anomalies are separated from the background of the wafer through a series of statistical models, edge detection, blob recognition algorithms, and color processing. The process allows the edge inspection module to detect artifacts on the wafer edge or edge top that are distinguishable from the background by their color, brightness, or shape. The edge inspection module provides edge exclusion detection using both bright-field and dark-field illumination.

A unique automatic focus-tracking technique allows the edge inspection module to keep the entire wafer edge surface in focus as the wafer rotates 360 degrees, as shown in Figure 2. The system passes the images through an algorithm that detects defects in the normal face of the wafer.

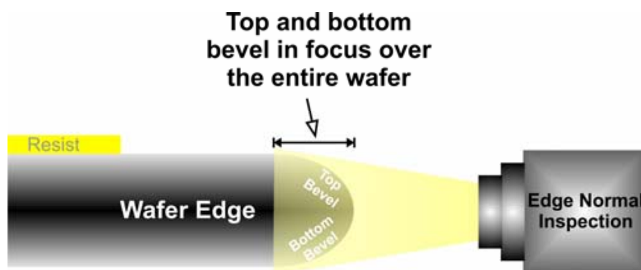

Figure 2. Keeping the edge and bevel in focus

REPEATABILITY TEST

To characterize the performance, repeatability, and reliability of the E20, we selected several 300mm wafers for the E20 to inspect over 10 runs. The wafers had approximately 100-200 defects on the edge normal, and 20-50 defects along the top edge. We set the edge top inspection width to 0.9mm.

Figure 3 illustrates the repeatability of the E20 in detecting edge top defects. On average, the E20 detected 60 percent of the defects.

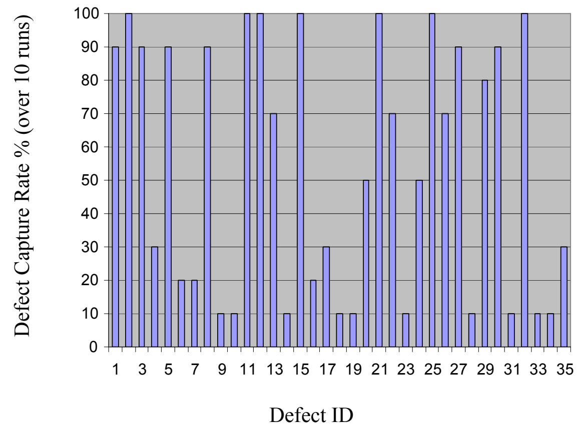

Figure 3. Edge top defect repeatability

Figure 4 illustrates the repeatability of the E20 in detecting edge normal defects. On average, the E20 detected 83 percent of the defects.

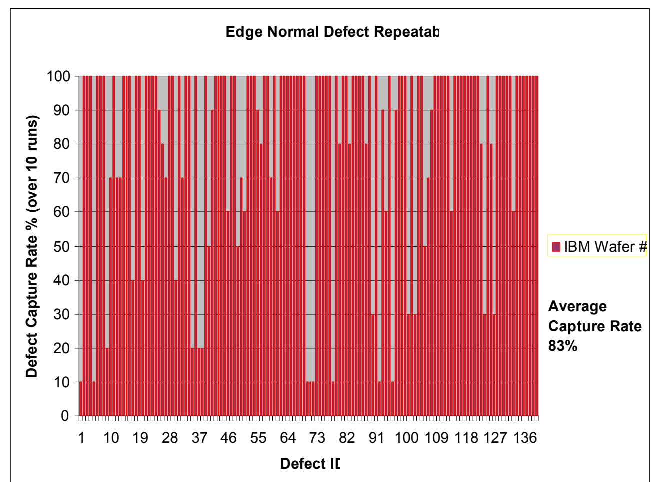

Figure 4. Edge normal defect repeatability

The repeatability of edge defect detection depends primarily on the level of contrast between the defect and the wafer surface. However, large variations of the edge band can also impact inspection repeatability. For instance, Figure 5 shows an image of a wafer edge. The degree of variation of the edge band causes lower defect repeatability since the size of the region of interest is not consistent along the edge.

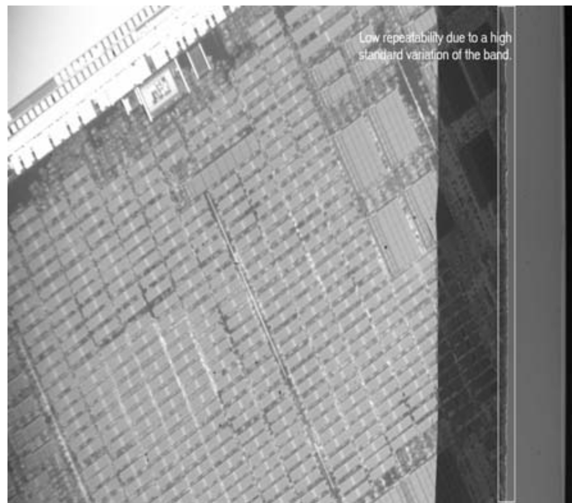

Figure 5. High variation of the band causes lower defect repeatability

Figure 6 shows an image with two defects with high repeatability rates—even though the defect in the bottom right corner is on the edge. The tool could easily find these defects due to the level of contrast between the surface and the background brightness.

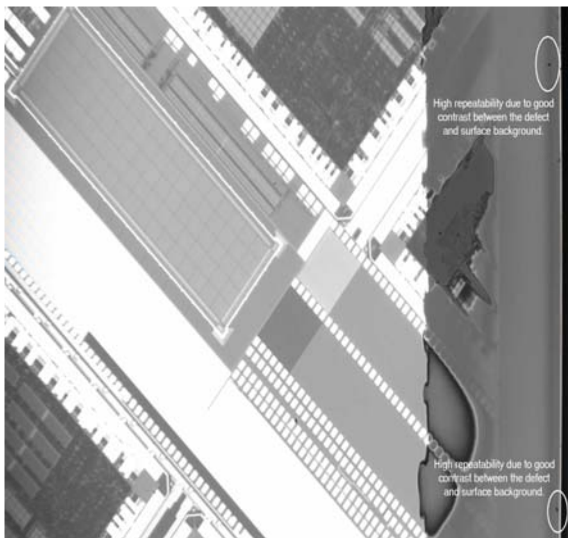

Figure 6. Defects with high repeatability on the top edge

Figure 7 shows an image of defects with high and low repeatability along the edge normal. The defect on the left has poor repeatability due to a low level of contrast between the defect and the wafer surface brightness and color. The defect on the right is more repeatable since there is more contrast between the color of the defect and the wafer surface.

Figure 7. Defects with high and low repeatability along the edge normal

THE EXPERIMENT

We selected a volume production 130nm technology node to begin wafer edge inspection tests. The integrated system would sample less than 10 percent of split 300mm wafers from various lots to identify defect counts after each process. Defect data showed that the last Cu CMP metal and M5—which is the next to the last back-end process—exhibited the highest level of bevel defects. Even though we could not observe particles flaking or pealing off from the edge, we suspected the defects were a result of the thick film and plating processing pealing or flaking off.

Figure 8 is an image of a wafer from the process of record that shows the bevel film colors on the bottom bevel. Notice the discontinued or partially delaminated films surface on the top bevel, along with residual Cu on the very top of the bevel. The wafer's total bevel defect count is 112.

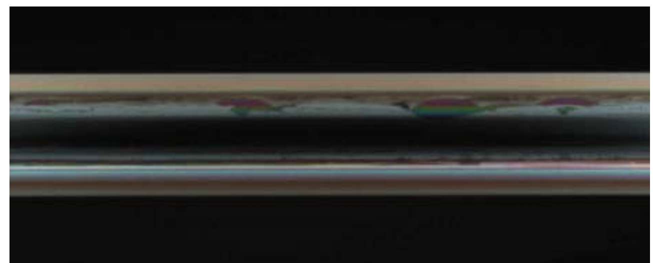

Figure 8. Bevel image of process of record wafer with no bevel clean. The total bevel defect count is 112.

Since a significant number of defects surfaced after Cu CMP, we next ran split 300mm wafers with a chemical bevel clean after Cu plating (pre-Cu CMP) and the last Cu CMP. We setup the tool to inspect the bevel during post-Cu CMP.

Figure 9 shows an image of the same wafer edge (depicted in Figure 8) after the post-CU CMP bevel clean. The extra clean process removed 76 of the 112 defects—bringing the total defect count down to 36.

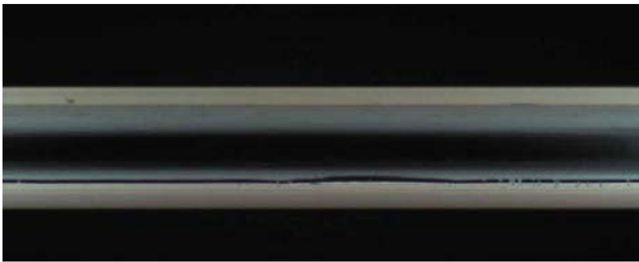

Figure 9. Bevel image of wafer with bevel clean. The total bevel defect count is 36.

We also performed cleans after M1 and M2 to evaluate their impact. However, inspection data revealed that defect counts were not significantly affected.

RESULTS

Figure 10 compares the average defect counts from the process of record inspections and processes with a bevel clean. The chart shows that there are over 100 more defect counts on the process of record wafers than the split bevel clean wafers.

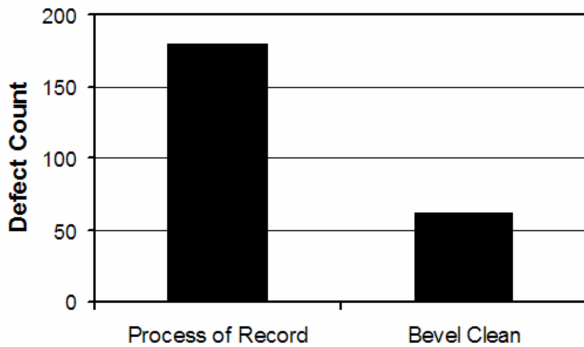

Figure 10. Bevel inspection average lot defect count

Although we could not observe edge conditions causing defects on the topside of wafers, the experiment results proved that higher defect counts on the bevel correlated to a degradation in wafer final test yields.

Figure 11 shows the yield improvements from split lots run in manufacturing through wafer final test. The wafer final test was performed after passivation, before dicing. A total of 3103 wafers ran through the process of record (without a clean) and 503 wafers ran with a bevel clean. The figure shows that the bevel inspection and clean process improved wafer final test yields by ten percent.

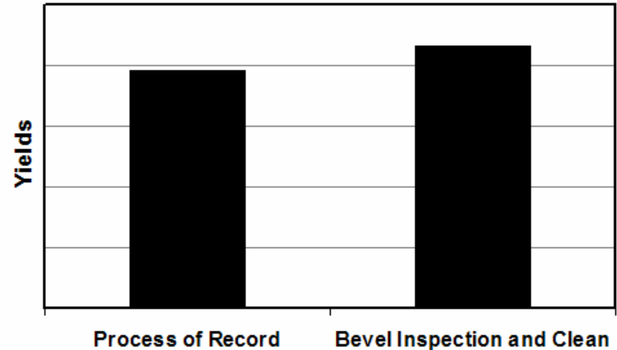

Figure 11. Wafer final test average yield improvements

The experiment proved that a bevel clean should be performed only after specific processes. The automated macro inspection tool collected the data required to maximize the capacity for cleans. We updated the process of record in the 130nm process and the 90nm process nodes to include the bevel clean after Cu plating, and after the last Cu CMP. By implementing the bevel cleans, we improved our yields by 10 percent.

We are now using the edge inspection tool to conduct other experiments. For instance, we are monitoring the edge on limited samples to determine how a double scrubber tool in CMP changes yields. We are also planning to inspect a sampling of wafers to determine whether there is a correlation between edge bead delamination and yield-inhibiting defects. Ultimately, we will be using the advanced macro inspection tool to perform an all-surfaces inspection within one manufacturing operation step.

ACKNOWLEDGMENTS

Thanks to Ann McDonald for her tireless help in splitting production wafers for bevel inspection and clean.

REFERENCES

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