Advanced Macro Inspection Provides Data to Address Blister Defects

Randy Smith*[a], Sean M. Collins*[b]
[a]August Technology, 4900 West 78th Street, Bloomington, MN, USA 55435;
[b]Texas Instruments Inc., M/S 3707, P.O. Box 650311, Dallas, TX, USA 75265

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ABSTRACT

This paper describes a method for automatically inspecting the top edge region of a wafer for defects and how this method was used to evaluate process improvements. The need for such an inspection was driven by a wafer defect problem first seen on product. The root cause of the defect was found to be the redistribution of certain defect types from the wafer edge exclusion region into the product area. Process partition and manual SEM inspection revealed the mechanism to be the formation and rupture of blisters during part of the process sequence. These blisters were found to be as small as 2μm and appeared along the top edge of the wafers. During processing, a high percentage of these blisters would rupture and redeposit debris on the topside of the wafer resulting in a nearly 100 percent kill rate. While the root cause was understood, the use of SEM inspection to quantifiably evaluate process improvements intended to reduce the edge defects was impractical. This was deemed impractical because of the large number of wafers required to generate meaningful statistics and the number of process options. In addition to this, manual inspections used to count the number of defects were inconsistent as well as slow. An automated macro defect inspection system (August Technology AXi-930) was used in a novel way to enable fast, accurate, and repeatable defect counts from the wafer top edge to help determine the most appropriate process improvement.

Keywords: Edge, Defects, Blisters, Inspection, Semiconductor, Process Development

1. INTRODUCTION

As part of yield ramp activity at Texas Instruments it was discovered that certain embedded defect types were found in much higher numbers on product compared to single process unpatterned monitor wafers. By utilizing unpatterned short flow wafers the defect type and number was reproduced. Manual SEM inspection of this short flow revealed blisters as small as 2μm. These were found only on the top edge of the wafer in a region uninspected by any unpatterned wafer inspection tool. The blisters formed on the polished surface of the wafer close to the transition of the wafer bevel. The defects were not in a continuous band but found in isolated locations both intact and ruptured. An example of both types is shown in an image taken with a scanning electron microscope (SEM) in Figure 1.

When the blisters "popped" during part of the process, dielectric debris was scattered and redistributed randomly across the wafer. Because of the size and timing of this event, the kill rate for these defects was nearly 100%. Although manual inspections on the SEM and optical microscope were used to understand the defect mechanism, an automated means of inspection was needed to enable quick evaluation of process complex improvements.

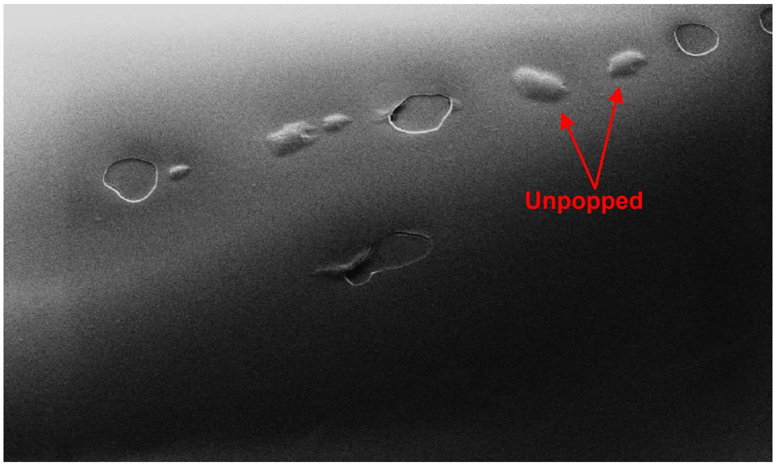

Figure 1: Blister defects captured by a SEM

An August Technology All Surface Wafer Inspection tool is under evaluation by Texas Instruments. The tool is located in KFAB in the Kilby Center, on TI's North Campus in Dallas. This tool is composed of an AXi-930 macro module, an E20 edge inspection module and a B20 backside inspection module. These are integrated on an UltraPort wafer handling module. Part of the methodology of the tool evaluation is to understand how it performs solving real life problems in addition to other standardized testing. The edge defect issue described above was used as one means of evaluating this tool.

2. METHODOLOGY

Though the tool has a specific edge inspection module the 2µm defects we were concerned with for this project were outside the designed sensitivity of the E20. Though not intended to perform an edge inspection, the macro module had the flexibility to perform the inspections required within certain limitations.

To perform the top edge inspection using the AXi-930 the recipe was set to inspect a pseudo die pattern along the edge of the wafer with two or three die per row. The coverage of the inspection was only a small percentage of the wafer surface. Specifically, the region of interest included the bevel transition and 2-3 mm of the top edge. In order to completely cover the region of interest, the setup included the inspection of areas partially off the wafer. Rough binning of defects allowed false defects detected on the bevel and off the wafer to be completely disregarded. System magnification was set at 5X to detect defects as small as 2µm.

One feature that was employed extensively was automatic defect review at a magnification higher than the inspection magnification. Automatic review at 20X magnification was added to the inspection recipe as a standard part of the inspection. The inspection setup provided a throughput of 30 200mm wafers/hour including high-resolution image capturing of each defect per wafer.

The use of the inspection was limited to unpatterned pilot wafers. The complex nature of this region on patterned wafers, with partial die shots, color variations and artifacts from edge treatments, is beyond the technology for 2µm sensitivities.

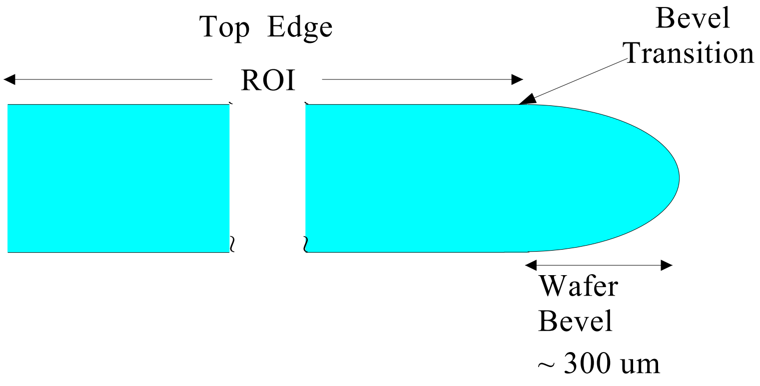

Figure 2: Region of interest along the edge

The inspection described above was used as part of the methodology to determine the most effective means of eliminating the blister defect. Unpatterned short flow lots would be split to evaluate various process alternatives. Each wafer was inspected using both the standard unpatterned defect inspections to characterize the within wafer defectivity and then with the edge inspection to characterize the edge defectivity.

Typically the first inspection was on the starting material and then again up to five inspections per wafer, one for each subsequent process step. Then because of the complex interactions between the processes involved, performing inspections after each step was necessary to develop a solid understanding of the impact of each process option. The high resolution images automatically captured during the inspection aided in the overall understanding of the impact. Typically, images of the four largest and four smallest defects on each wafer were collected. Defect coordinates, sizes, and high magnification color images were automatically recorded and stored on an off line yield enhancement database for later data analysis. A sample wafer map is shown in Figure 3.

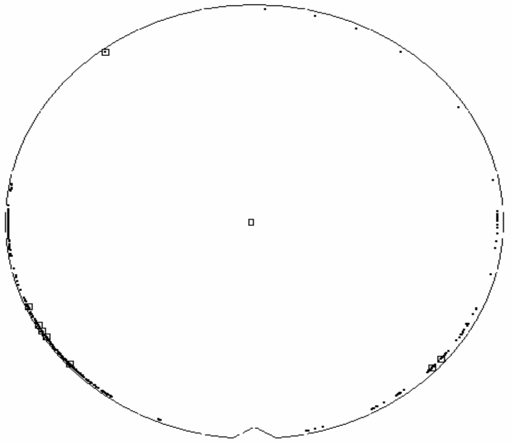

Figure 3: Edge inspection wafer map

3. DATA

Over a three month period, a total of 446 wafer edge inspections were performed as part of this project. Figure 4 illustrates typical edge inspection results from one of the process partitions. Using automated edge inspection allowed the effective numerical evaluation of process alternatives. The chart shows the defect counts on the wafer edge for three short flow wafers and how the number of edge defects change at each step. Additionally, the inspection provides an understanding of the defect signature on the wafer and what impact a process change may have.

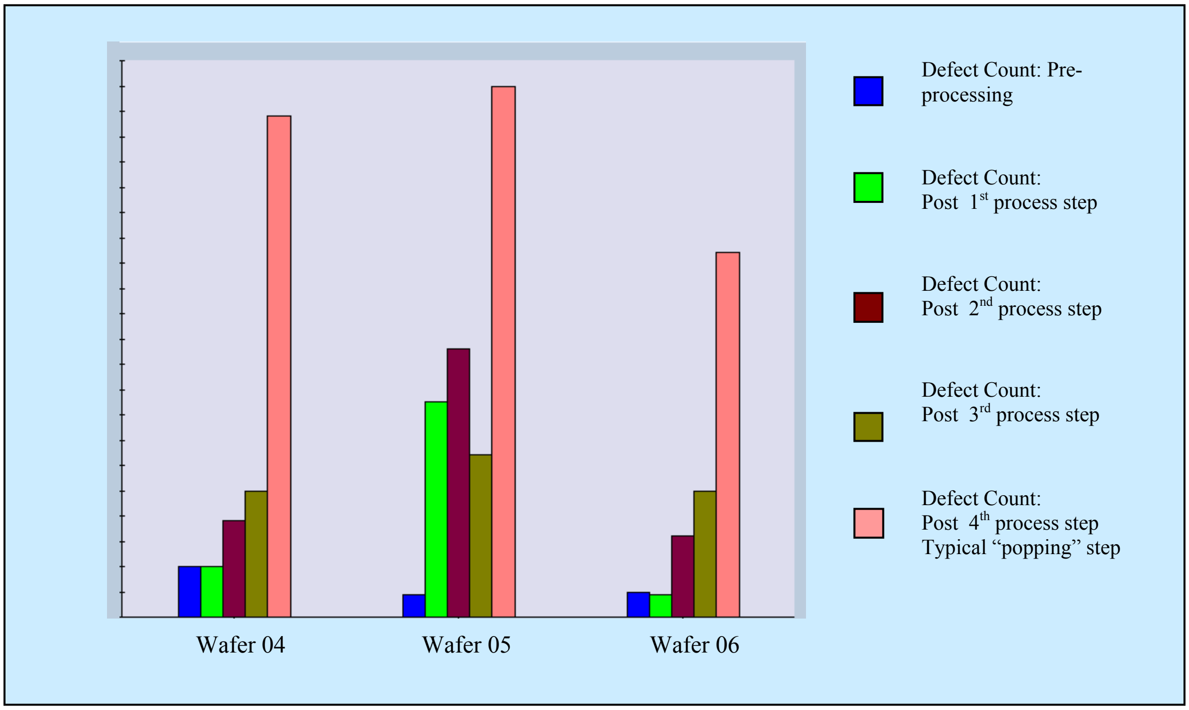

Figure 4: Short Flow Split Lot Analysis

High-resolution images, shown in Figures 5, 6 and 7, allow for further analysis of process changes and their affect on the defect transition from one step to the next.

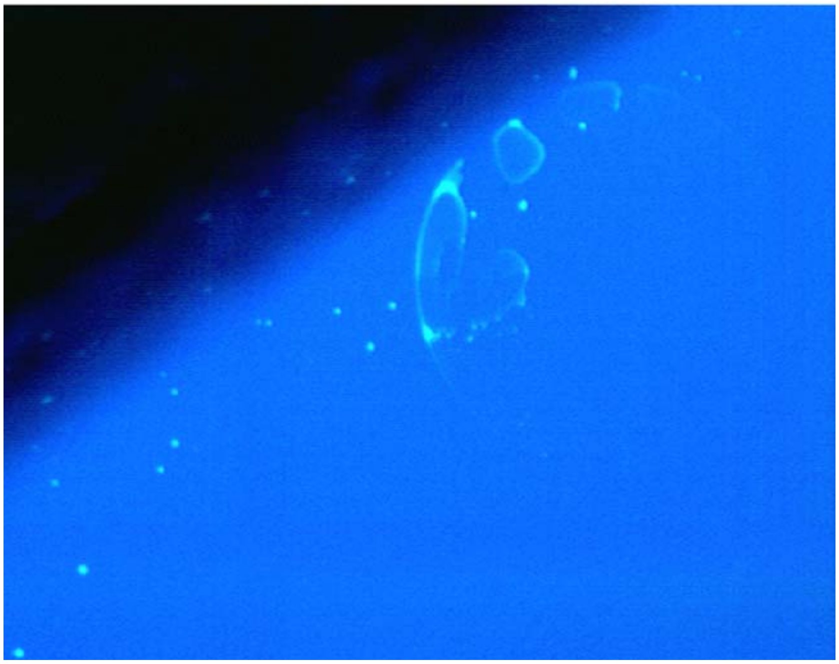

Figure 5: Blister defect at 20X magnification

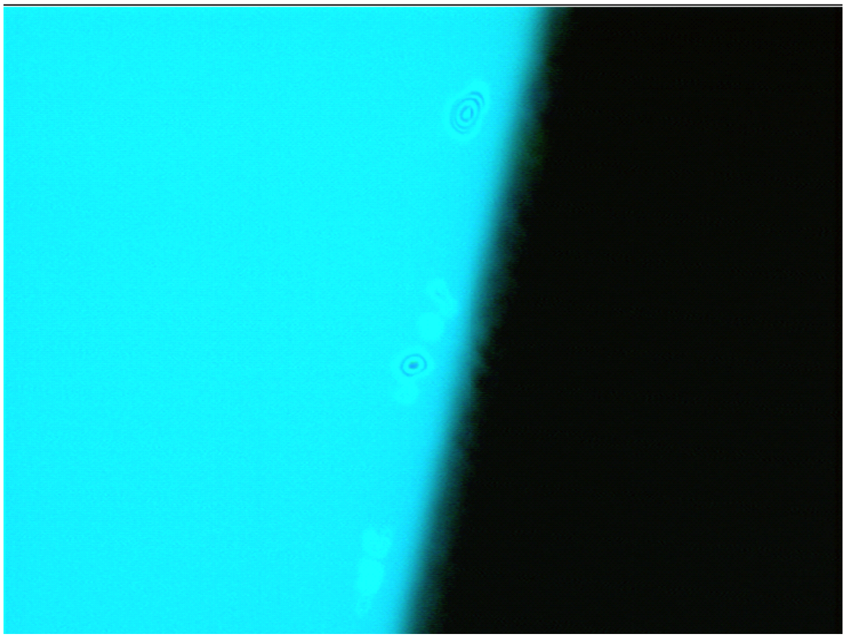

Figure 6: Top edge with blister defects

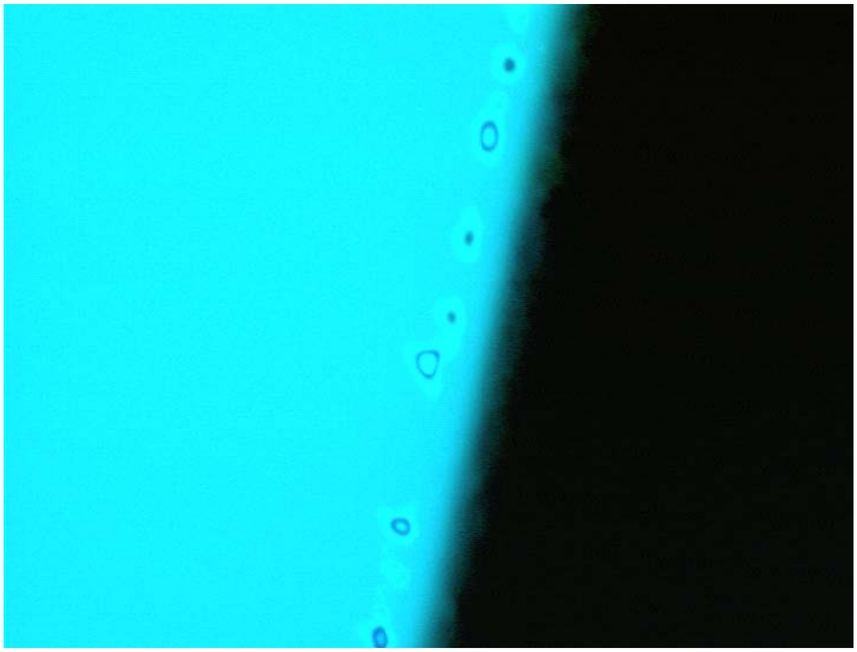

Figure 7: Top edge with blister defects

4. CONCLUSION

Using automated edge inspection can greatly enable yield learning on short flow wafers when complex defect mechanisms are involved. The inspection sensitivity required on top edge is smaller than previously thought and is at least 2µm. The complex structure of the top edge on patterned full flow wafers presents a unique challenge to effectively detecting defects of interest from background surface features.

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REFERENCES

*randy.smith@augusttech.com; phone 1 512 923-2397
*seancollins@ti.com; phone 1 972 927-6040