APPLICATION NOTE

All-surface Inspection for 3D-interconnects and TSV Manufacturing

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ABSTRACT

The need to inspect the topside, edge/bevel and backside of wafers at various stages of the semiconductor manufacturing process has been driven by device manufacturers continuing the push to 100% wafer-surface utilization for active die. As a result, the wafer-edge exclusion is becoming a thing of the past. With requirements for improving yield, thereby reducing costs, coming to the forefront, processing challenges are simultaneously increasing. The effect of adding knowledge about topside, bevel and backside-specific process phenomenon can be utilized not only in killer defect detection, but also in process improvement that ultimately drives yield improvement.

Once-new processes such as immersion lithography and deposition of high-k dielectric films have driven the development of wafer edge inspection technologies. As these processes become mainstream to semiconductor manufacturing, the next big drivers for continuous improvement in inspection and metrology equipment (and the application of that equipment) will include the 3D-interconnects (3DIC) initiatives. Interconnects are one of the industry's most difficult challenges: they involve depositing metal into deep and narrow microscopic holes etched into a chip. 3DIC has specific needs for yield-enhancing information and analysis which can be addressed by the next generation of all-surface inspection equipment.

Wafer-Level and Chip-Scale Packaging brought the concept of re-introducing a "back-end wafer" back into the front-end process for RDL deposition and subsequent steps, and this is being seen again in the 3DIC/TSV development path. There is much key learning in inspection and metrology that can be applied to these parallels, which if shared and applied correctly will result in a shorter learning curve as 3DIC/TSV processes become standardized.

INTRODUCTION

3D interconnects are important because of the push towards faster, more functional devices that are simultaneously smaller, and more power efficient. Connecting chips with discrete functions in a highly parallel way, and using the same PCB real-estate is the end goal. For example, by integrating memory above a processor die with a 1,000 "pins" (or TSVs) parallel connection can reduce power consumption in the interconnect to less than 1/10th that of a conventional interconnect.[1]

TSVs may be the vehicle the industry uses to extend Moore's law by allowing us to sidestep the issue of shrinking the transistor pitch altogether. TSVs promise the best advantages of System-on-Chip (SoC) and System-in-Package (SiP) together while achieving the optimum balance of functionality, low cost, and the shortest time to market among all serious alternatives.

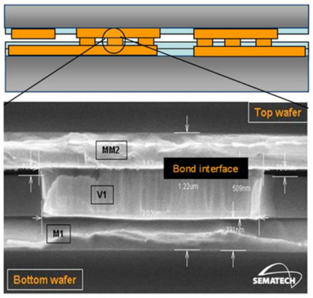

Figure 1 - TSV cross-section (SEM image)

Through-Silicon Vias (TSVs) will be the 3D interconnects' method of choice for future generations of devices because of the many advantages offered, chief among them being the higher densities of interconnects possible. This results in faster devices with lower power consumption. There is also the ability to manufacture the interconnects in-situ or along with die level packaging processes, instead of requiring separate device-level integration at wire bonding.

This paper discusses the applications for inspecting all surfaces of semiconductor wafers during various steps in the 3D interconnects and TSV manufacturing cycle. Inspections were performed on a Rudolph Technologies AXi™-935 E30/B30 Advanced Macro-Defect Inspection system at SEMATECH's wafer-to-wafer (WtW) 3D interconnect line at the College of Nanoscale Science and Engineering (CNSE), University at Albany, State University of New York (SUNY). Examples of inspections taking place on the front, edge/bevel and backside of the wafer will be shown and the potential yield saving impacts discussed.

The main purpose of this paper is to serve as an exposé of some of the automated inspection applications available for 3D interconnects manufacturing, in order to generate discussion on the creation of standards and best-practices. Consequently, this paper does not feature specifications of repeatability/reproducibility data for any particular piece of equipment that is being put forward, or any specific or proprietary yield data from a manufacturing line.

BACKGROUND

SEMATECH's 3D program is geared towards delivering through-silicon-via manufacturing technology to member companies. The goals of the program are to: 1) put into place a set of 3D specific tools and leverage CNSE equipment set to have complete development and exploratory capability in 3D. 2) Evaluate the cost effectiveness and manufacturability of tools, materials, unit processes, integrations and metrology for 3D. 3) Deliver 3D processes, materials and integrations to meet the production requirements and timelines of the Member Companies. 4) Meet or exceed the ITRS TSV targets.

Through an associate membership, Rudolph has been able to work together with SEMATECH in the performance of the experimental inspections described in this paper. SEMATECH has brought several process modules on-line in 2009 and is working to finish the complete manufacturing line in 2010. Simultaneously, work has been on-going at Rudolph to develop TSV and 3D interconnects inspection techniques on currently available manufacturing processes.

INSPECTION THEORY

Inspection is distinct from metrology and suffers from more ambiguous definitions. To distinguish it from metrology, one definition holds that inspection is a qualitative process through which extrinsic attributes of a sample under study can be revealed, depending on the method and basic resolution of the equipment being used. Results can be measured comparatively against other results from a standard or "golden" wafer, but usually this is only done during periodic performance verifications. In semiconductor visual inspection the ultimate output of inspection results will be to determine what is "bad" and "good" based on a number of flexible variables that can be controlled by the equipment engineer. For instance, certain contrast levels or feature shapes. By allowing flexible and subjective variables to be defined which adjust the inspection results, automated inspection aims to replace manual inspection.

Metrology on the other hand, is defined as a measurement that is capable of giving a gauge-certified value in definite units when a specific feature or property is measured in a strictly controlled manner. The calibration of metrology equipment is not tied to just one proprietary "golden wafer", but rather to an established and universally accepted standard. Metrology also depends on definitive pass/fail criteria, while inspection implies subjective criteria.

Inspection on All-surfaces of the Wafer

While there are many unique and well-established technologies for automated inspection of the front-side of wafers, inspecting the bevel of the wafer is still a relatively new concept. Only a few examples exist of commercial tools marketed for bevel inspection. The need to inspect the bevel of wafers has only become apparent recently, thanks in large part to the challenges presented by control of defectivity in immersion lithography applications.

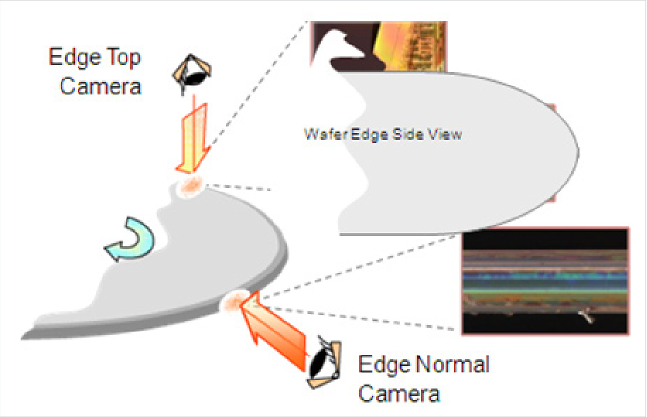

Figure 2 - Diagram showing perspective of edge top and edge normal cameras

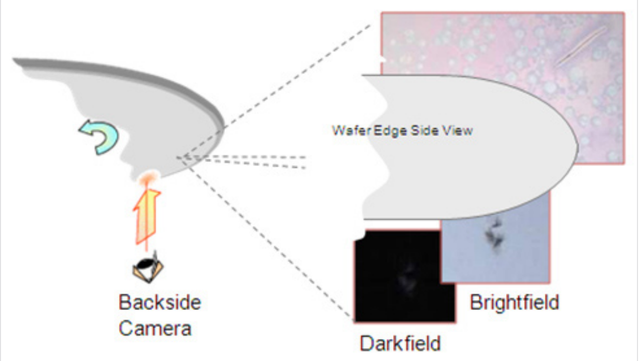

Figure 3 - Diagram showing perspective of backside camera

Bevel inspection is equally important to 3D interconnects manufacturing.

HANDLING OF BONDED WAFERS

Because the wafers are bonded during the 3D process, it is important that the equipment (including the robotic wafer handler) is able to handle a ~1550 micron thick wafer pair, equivalent to two standard SEMI M1 300 mm diameter wafers at 775± 25 micron total thickness each.[2] Because this is not yet common throughout the industry, we found that there were several challenges to be addressed specific to handling bonded wafers.

Adjustments to the cassette mapping were necessary so that the robot would not detect the wafers as a cross-slot or mistakenly double-slotted pair. In addition, robot speed was reduced until safe wafer handling could be assured. Because two wafers are twice as massive as one, robot end effector bow has to be monitored carefully.

INSPECTION EXAMPLES

Inspections were performed both for in-line manufacturing monitoring after various 3D interconnects , steps, and also as specifically designed experiments meant to test the capabilities of the equipment. Front, edge/bevel and backside inspection applications will be discussed.

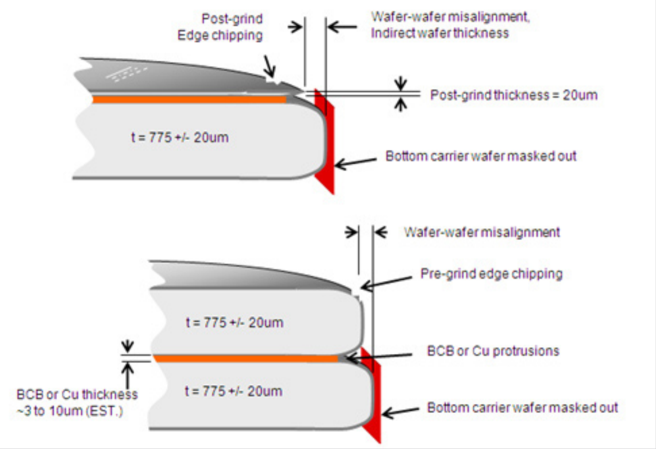

Figure 4 *- Attributes and defects in bonded wafer pairs*

Front Surface Inspection of Wafer After Wet Processing

A common application for the equipment is to inspect wafers for foreign material (FM) and other defects that may have been introduced during wafer processing. In one example, wafers that went through a wet process and were subsequently dried were found to have slight discolorations across the wafer that was assumed to be oxidation (figure 5). This may have been induced by the process itself or by storage methods used for these wafers.

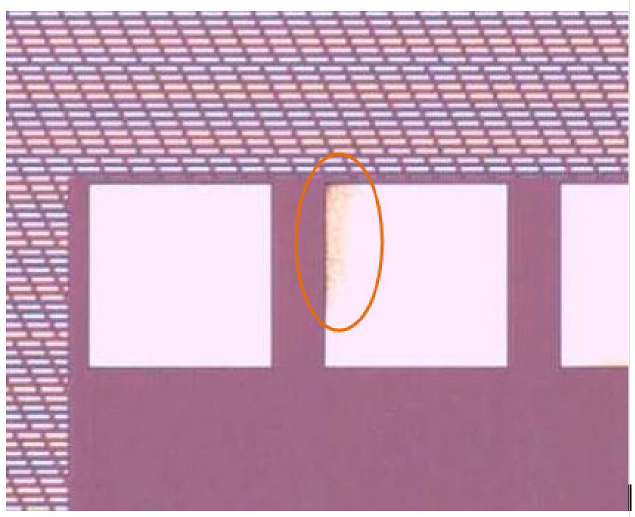

Figure 5 *- Automated inspection after wet process revealed oxidation on metal traces.*

Discovering these defects resulted in savings associated with avoiding further wafer processing and potentially more costly rework later. These defects would most likely not be found using manual inspection.

Edge-bevel Inspection of Bonded Wafer Pairs

The edge inspections are performed by a dedicated module that is part of the cluster and has the independent cameras for edge top (ET) and edge normal (EN) shown in figure 2. As well as having independent cameras, two sources of illumination are available for each camera. High scattering defects in partially patterned and non-patterned ET areas can be detected by using darkfield (DF) illuminations and algorithms. A low grazing angle is used to illuminate the defect without illuminating the underlying patterns and to detect defects based on scattering intensities. Once detected, the system marks the location of defects for later color image capture in brightfield (BF) illumination.

To verify the bond process, inspections were performed after wafer bonding, and before thinning of the top wafer. This method allowed process problems to be caught before subsequent steps were performed on wafers which had bonding problems.

In the bonding process there is a chance for foreign material (FM) to be introduced into the bond area, or between the wafers. FM in this area may have become lodged and may be difficult to remove through conventional cleaning techniques (figure 6). FM in this area may lead to voids in between wafers which result in electrical opens.

Figure 7 *- Wafer edge chipping on the bevel. Image captured in DF illumination.*

Wafer edge inspection is also of critical importance in detecting wafer damage which may result in costly equipment downtime due to subsequent wafer breakage. Handler-induced edge chips (figure 7) have been found to later cause wafer breakage due to brittle fracture. Good separation of the BF and DF channels is critical to isolate the detection of this type of defect. An edge chip can be seen clearly in DF while the color noise from the BF channel does not interfere with detection.

Edge-Top Inspection of Wafer After Trimming Process

As the wafer edge becomes very thin - like a knife edge - during grinding, it has a chance of breaking. To avoid this, the top wafer can be trimmed prior to the thinning step (figure 8). The edge trimming process can be monitored for process problems such as cracking or chipping.

Figure 8 *- Diagram of edge-trimmed, thinned wafer on carrier wafer.*

To inspect for defects in this edge trim zone only, a narrow region of interest should be defined so that other variations can be ignored (figure 9).

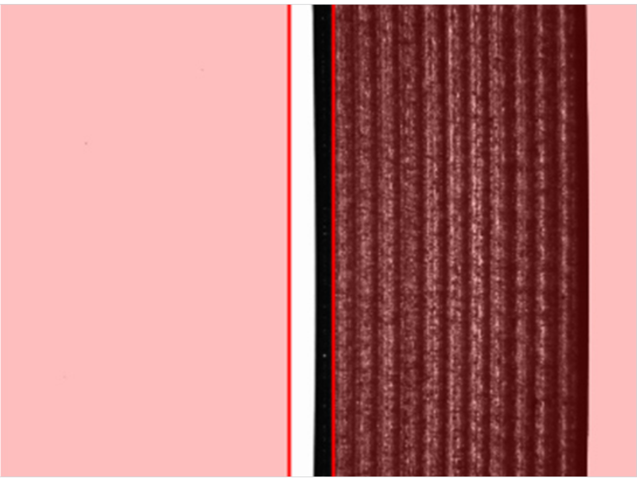

Figure 9 *- Region of interest showing the trim-line.*

Examples of defects of interest were found in some samples which provided evidence of an out-of-tolerance trimming process (figure 10).

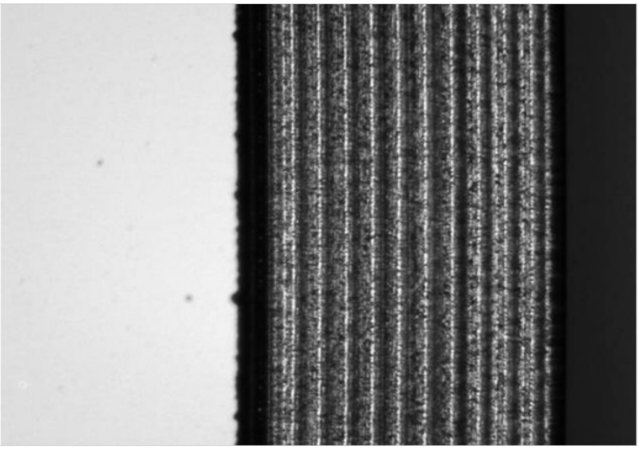

Figure 10 *- Defects on the trim line.*

Backside Inspection of Wafers in Bond Processes

The most often neglected area on a wafer is the backside. In typical wafer processing, the backside of a wafer has traditionally been considered of little importance. It is eventually ground away, and the fact that there are defects there during processing may be taken for granted. In 3D interconnects manufacturing the back of the wafer plays a more critical role because of the depth and complexity of the processing steps which often involve wafer flipping. It is also safe to assume that 3D interconnects processing requires at least several times as much handling of the wafers themselves, and so the opportunities for defects to be introduced are multiplied.

During inspection of sample wafers, many different types of defects were found. Because standard requirements for the backside of the wafer are not well defined, the challenge is to determine which defects are critical and which are unimportant (figures 11 and 12).

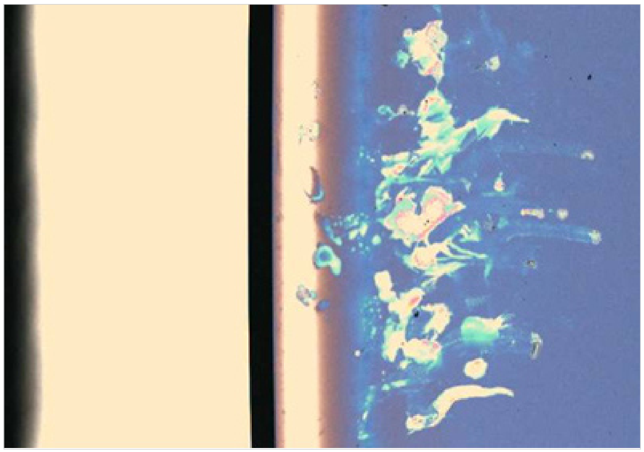

Figure 11 - Residue on the backside of a wafer.

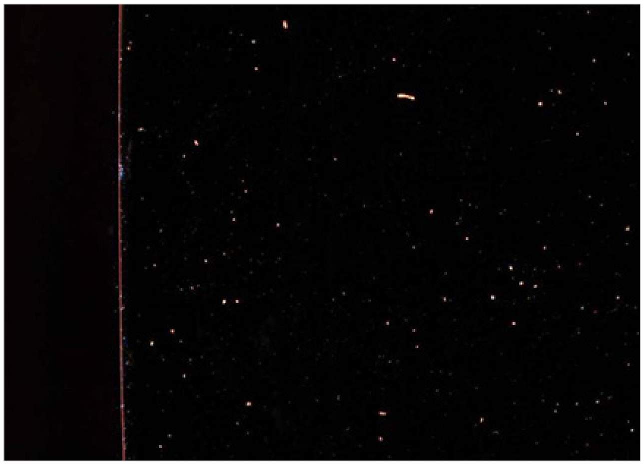

Figure 12 - Foreign material and possible scratches on the backside of a wafer. Image captured in DF illumination.

SUMMARY

This paper demonstrated the value of performing in-line automated inspections during 3D interconnects manufacturing by showing that key defects of interest are captured after various processing steps. The bonding of wafers, and the unique challenges that accompany it, are unique to 3D interconnects and demand new equipment and new methods to address the emerging inspection and metrology requirements.

The fact that these wafers must be re-introduced to "front-end" processes in via-first and via-middle applications makes the case for in-line inspection even more clear, and draws important parallels between the challenges shared by 3D interconnects manufacturing and Wafer-Level Chip-Scale Packaging (WLCSP).

FUTURE WORK

Future work at SEMATECH will include work on inspection and metrology requirements for die-to-wafer (DtW) integration, and further work to help define standards and best practices for in-line inspection and control of 3D interconnects manufacturing as a whole.

ACKNOWLEDGEMENTS

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